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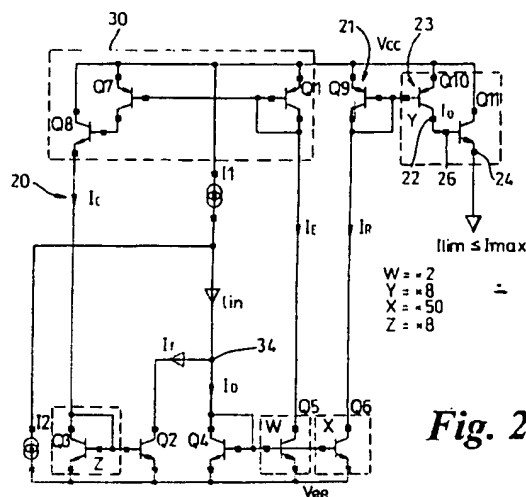
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(54) Driver circuit for a solid state optical emitter device

(57) The present invention relates to a circuit for driving a solid state optical emitter device such as a laser diode, and in particular a circuit which limits the maximum current which may be drawn through the device. The circuit comprises a current supply path and a current return path to which the optical emitter may be connected, and current limit means (20) to limit a maximum current (I_{max}) that may flow through one of the current paths. The current limit means (20) has a current mirror with an input portion (21) and an output portion (23), the circuit being arranged so that when a first current (I_R) flows through the input portion (21) the second portion (23) is predisposed to supply a second current (I_o) up to a maximum which mirrors the first current (I_R). The maximum current (I_{max}) through the paths is thereby limited in accordance with the maximum of the second current (I_o).



Description

[0001] The present invention relates to a circuit for driving a solid state optical emitter device such as a laser diode, and in particular a circuit which limits the maximum current which may be drawn through the device.

[0002] Laser diodes are used in many devices, such as in optical data storage read/write heads, fibre optic transmitters or hand-held pointers. It is usually the case that the permissible maximum power output by the laser diode must be limited, either for eye-safety or so that the device will work correctly. The actual current limit will depend on the type of laser diode and the application in which it is used, but in most cases the current limit will be of the order of about 100 mA.

[0003] One way of monitoring the current sourced by the laser diode is by measuring a voltage generated across a resistor in series with the laser diode. This approach suffers from several disadvantages. One is that power is wasted through the resistor, which can be a concern with battery powered devices. Another is that the voltage drop across the resistor necessitates a higher supply voltage, and in some applications it is desired that the supply voltage should be as low as possible. A resistor voltage is then monitored by a circuit, and often this circuit may be connected to a separate circuit to check that the monitor circuit is working properly. This adds cost and complexity to the monitoring circuit.

[0004] According to the invention, there is provided a driver circuit for a solid state optical emitter, the circuit comprising a current supply path and a current return path to which the optical emitter may be connected, and current limit means to limit a maximum current that may flow through one of the current paths, characterised in that the current limit means has a current mirror with an input portion and an output portion, in which the circuit is arranged so that when a first current flows through the input portion the second portion is predisposed to supply a second current up to a maximum which mirrors the first current, the maximum current through the paths being limited in accordance with the maximum of the second current.

[0005] The optical emitter device may be a laser diode, a light emitting diode, or other such solid state device operating, for example, in the infrared or visible parts of the spectrum.

[0006] In most cases the return path leads to a ground, and the supply path come from a positive supply voltage. The greatest risk of supplying too much current to the optical emitter will normally come from a short circuit. For example, in the case of a laser diode, this will normally be the risk of a short circuit between the laser diode cathode and ground. Therefore, it is usually preferred if the current limit means is provided in the supply path.

[0007] The output portion of the current mirror may be

in series with the optical emitter device, in which case the current through the device, and hence the current through the supply and return paths, will be directly limited to a maximum corresponding to the maximum current that may be supplied by the output portion of the current mirror. In this case, the current through the paths is limited to a maximum which mirrors the first current.

[0008] Alternatively, the maximum current through the paths may be limited indirectly by the current through the output portion of the current mirror. For example, the current from the output portion may be fed to a gating means such as an amplifier circuit or the base of a transistor which may have a higher current rating, than the current mirror. Such a transistor is then gated up to a maximum current by the current through the output portion of the current mirror. In this case, the current through the paths is limited to a maximum which is a simple multiple, divisor or other function of the first current.

[0009] Because transistors typically have a large variation in gain between production batches, but nearly identical gain within the same batch or on the same chip the circuit preferably comprises signal generation means such as feedback means to compensate for gain variability of the gating transistor.

[0010] Often, the laser will need to work over a range of operating conditions and may be pulsed at a varying duty cycle. The circuit may therefore comprise signal generation means to compensate for temperature variability of the laser diode optical power versus temperature characteristic.

[0011] In a preferred embodiment of the invention, the first current through the input portion of the current mirror passes through at least one transistor which is gated by the signal generation means.

[0012] It will generally be the case that the current return path has laser diode bias control means to set a bias current through the laser diode. When the laser is to operated in a pulsed mode, the current return path may have a laser diode modulation means to modulate the current through the laser diode.

[0013] Also according to the invention, there is provided a method of driving a solid state optical emitter with a circuit comprising a current supply path and a current return path to which optical emitter may be connected, and current limit means to limit a maximum current that may flow through one of the current paths, characterised in that the current limit means has a current mirror, comprising the steps of:

i) generating a first current in an input portion of the current mirror;

ii) predisposing an output portion of the current mirror to supply a second current up to a maximum which mirrors the first current; and

iii) using the maximum second current to limit the maximum current through the paths.

[0014] The invention will now be described by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a conventional arrangement for driving a laser diode, with laser bias and modulation control and a current limitation circuit; and

Figure 2 shows a current limitation circuit according to the invention, for use as part of a laser diode driver circuit.

[0015] In Figure 1, a conventional laser diode driver circuit 1 has power supply lines Vcc at +5 Volts and Vee at 0 Volts. A connection 2 is made from Vcc to a conventional current monitor circuit 4 having, for example, a low value resistor (not shown) for generating a voltage representative of a current Ilim supplied from line Vcc. The current Ilim flows from the current monitor circuit 4 through another connection 6 into the anode of a laser diode 8. From the laser diode cathode, Ilim is split by connection 10 through two parallel npn transistors Q_M, Q_B as Ilim flows through connections 12 to Vee. Q_B is driven to bias the laser diode to the base of its operating point, and Q_M is then driven according to the desired modulation of the laser diode.

[0016] Therefore, the circuit elements 2,4,6 define a current supply path to the laser diode anode, and the circuit elements 10,Q_B,Q_M,12 define a current return path from the laser diode cathode.

[0017] Depending on the bias and modulation drive, Ilim may take any value from 0 to I_{max} mA, where the circuit is designed so that in normal operation of Q_B and Q_M, I_{max} is within a tolerable limit, defined for example by the need for eye safety, or by the maximum rated output of the laser diode 6.

[0018] If a fault develops in Q_B or Q_M, or if a short circuit is formed from the laser diode 8 cathode to Vee, then the current through the laser diode could exceed I_{max}. Consequently, it is usual practice to include the current limitation circuit 4 which includes feedback circuitry to limit Ilim to the maximum value I_{max}.

[0019] When the laser 8 is to be operated in a pulsed mode, for example at up to a 50% duty cycle, then the current limitation circuit is normally designed to limit an expected mean Ilim. In some applications, for example fibre optic transmission or optical data storage, the expected current limit will be approximately 100 mA. Particularly in fibre optic transmission, there is a need for high frequency operation, for example of the order to up to 2 GHz with commercially available devices. These current and frequency requirements place constraints on the type of current limitation circuitry which can be employed.

[0020] In order to guard against a fault in the current

monitor circuit 4, a separate monitoring circuit (not shown) is sometimes used to monitor the performance of the current monitor circuit 4, adding cost and complexity to the laser diode driver circuit 1.

[0021] Figure 2 illustrates a current limitation circuit 20 according to the invention, which may be used in place of the conventional current limitation circuit 4 of Figure 1. The circuit 20 is an integrated bipolar device with a current mirror consisting of two pnp transistors Q9,Q10. In comparison with equivalent npn transistors, pnp transistors are, of course, noted for lower current rating and lower frequency response. Although discrete components have higher ratings, a typical pnp integrated bipolar pnp transistor is limited to supplying about 200 μ A, with a maximum frequency response conventionally believed to be approximately 400 MHz. A generally useful laser diode current limitation circuit normally needs current and frequency response in excess of these limits.

[0022] The pnp transistor Q9 and eight parallel pnp transistors Q10 are, respectively, in an input portion 21 and an output portion 23 of the current mirror. A reference current I_R of the order of about 200 μ A is sunk from the input portion transistor Q9 through two parallel gating transistors Q6. Each transistor Q10 in the output portion 23 is therefore predisposed to supply the same current 200 μ A as an output current I_O to the base of an npn transistor Q11, which acts here as a gating transistor. Assuming a typical gain β of about 50 for such an npn transistor, the maximum total current I_{max} that can be supplied by the eight transistors Q11 to a laser diode is about 80 mA. If greater current is needed, then the number of transistors Q10,Q11 in parallel may be increased. Such an increase in the number of components is readily achievable in an integrated bipolar device. In fact, the number of pnp output portion transistors Q10 in an integrated device could readily be increased to the point where the total output portion current was sufficient to supply the laser diode directly. In this case, it is possible to dispense with the npn transistor Q11. It has been found in practice that in this circuit, the frequency response of the integrated pnp output transistors does not in fact limit operation to 400 MHz, as operation up to 2.5 GHz is possible. It is believed that this is due to capacitive coupling from the pnp collector to the emitter permitting current to flow. If needed, frequency response above about 2.5 GHz may be extended, for example up to about 25 GHz, by placing a coupling capacitor in parallel with the transistors Q11, between Vcc and pnp collector node 22. However, as explained below, it is preferred to use the npn transistor Q11.

[0023] If the bias and modulation for the laser diode is such that less current Ilim is pulled through the bias and modulation transistors, then the voltage at the emitter 24 of transistors Q11 will rise above that present at the base 26, until the base-emitter current I_o drops to a level consistent with the current pulled through the laser

diode. The relatively small base-emitter current in transistors Q11 is added to the main collector-emitter current. At the same time, the voltage at the collector 22 of pnp transistor Q10 rises above that of the base until the current I_0 supplied by pnp transistor Q10 is limited to that delivered to npn transistor Q11.

[0024] In both cases, with and without the npn transistor Q11, the arrangement is therefore such that there is a defined relationship between the input portion current and the output portion current. The output portion 23 is predisposed to supply a current up to a maximum which mirrors the current through the current mirror input portion 21, the laser current being limited to a maximum value according to the defined relationship with the current mirror input portion current.

[0025] The frequency response of the npn transistors approaches 25 GHz ($F_T = 1$), which is adequate for many uses of laser diodes. The frequency response of the pnp output portion transistor Q10, is of course lower than this level, but the base current into Q11 is essentially unaffected by such high frequencies, and will be limited when the average voltage at the npn emitter 24, and hence the voltage at the pnp collector 22 start to rise.

[0026] The other parts of the current limitation circuit 20 provide feedback useful in a commercial device. Portion 30 is duplicates the elements Q9, Q10, Q11 to compensate for the gain β of npn transistor Q11, which may vary between different production batches of integrated circuit. A current I_0 corresponding to I_{max} is fed into the input portion of an npn current mirror consisting of 8 parallel transistors Q3, thereby controlling an output current I_1 .

[0027] The current vs optical output characteristic of a laser diode is dependent on the temperature of the laser diode device, and this in turn is dependent on the ambient temperature. As ambient temperature increases, the optical output for a given drive current can increase or decrease, depending on the type of optical emitter device and temperature range. To achieve a broad band of ambient operating temperatures, it is therefore useful to compensate for this effect with an appropriate compensation signal from signal generation means to stabilize the optical output of the laser diode. In circuit 20, this temperature compensation is achieved using a well-known technique, in which the current I_2 from one current source is subtracted from a current I_1 from another current source to yield a resultant current I_{in} . The characteristics of the current sources I_1, I_2 can be chosen to provide the necessary temperature compensation characteristic in I_{in} .

[0028] The gain compensation current I_f is then subtracted from a current I_{in} at node 34 to yield a temperature and gain compensated current I_0 , which is input into an npn current mirror consisting of an input portion transistor Q4 and two output portion transistors Q5 and a further 50 output portion transistors Q6. The output portion transistors Q5 acts as a gating transistor to sink

the control current I_E from the input portion of compensating portion 30, and the output transistors Q6 act as gating transistors to sink the reference current I_R from the pnp current mirror input portion transistor Q9.

[0029] The behaviour of the circuit is therefore governed by the following equations:

$$I_{lim} = (I_{in} - I_f) \cdot X \cdot Y \cdot \beta \quad 1$$

$$I_f = (I_{in} - I_f) \cdot (W \cdot \beta / Z) \quad 2$$

[0030] Therefore, from equation 2:

$$I_f = (I_{in} \cdot W \cdot \beta) / (Z + W \cdot \beta)$$

[0031] Substituting I_f into equation 1 gives:

$$I_{lim} = I_{in} \cdot (X \cdot Y \cdot Z) / ((Z/\beta) + W)$$

[0032] If $Z/\beta \ll W$ then the Z/β term can be ignored.

$$\text{Gain} = I_{lim} / I_{in} = X \cdot Y \cdot Z / W$$

[0033] For $X = 50$, $Y = 8$, $Z = 8$ and $W = 2$, the gain would be 1600.

[0034] The circuit as described above may be used in a variety of applications, for example with an optical fibre transmission device comprising a laser diode and a laser diode driver circuit arranged to bias and modulate the laser diode. Other applications where the circuit may be useful include optical data storage read-write heads, laser pointer devices, and surveying equipment.

[0035] The circuit is particularly suited to integration using bipolar technology, but may be adapted to other types of integration, for example an integrated circuit comprising both biCMOS and bipolar transistors. In this latter case, the pnp current mirror could be replaced with a p-channel MOSFET current mirror. An advantage of p-channel MOSFETS would be a higher operating frequency, would may allow such a circuit to be used without the need for the current mirror to drive an npn transistor, so allowing the circuit to be somewhat simplified.

[0036] Although the invention has been described in detail as having the current limitation circuit in the current supply path, the invention is not so limited, and a current limitation circuit could equivalently be placed in the current return path leading from the laser diode cathode. In this case, the current mirror would be an npn current mirror, which would have the advantage of an inherently greater frequency response. Such an arrangement may be desirable if the packaging of the laser diode were such that there was a greater risk of a short circuit from the laser diode anode to V_{cc} , rather than from the laser diode cathode to Vee.

Claims

1. A driver circuit for a solid state optical emitter, the circuit comprising a current supply path (2,4,6) and a current return path (10,Q_B,Q_M,12) to which the optical emitter (8) may be connected, and current limit means (20) to limit a maximum current (I_{max}) that may flow through one of the current paths, characterised in that the current limit means (20) has a current mirror with an input portion (21) and an output portion (23), in which the circuit is arranged so that when a first current (I_R) flows through the input portion (21) the second portion (23) is predisposed to supply a second current (I_O) up to a maximum which mirrors the first current (I_R), the maximum current (I_{max}) through the paths being limited in accordance with the maximum of the second current (I_O). 5
2. A driver circuit as claimed in Claim 1, in which the current limit means (20) is provided in the supply path (2,4,6). 10
3. A driver circuit as claimed in Claim 1 or Claim 2, in which the current mirror is a pnp transistor circuit (21,23). 15
4. A driver circuit as claimed in any preceding claim, in which the maximum current (I_{max}) through the paths (2,4,6;10,Q_B,Q_M,12) is limited directly by the maximum current (I_O) through the output portion (23) of the current mirror. 20
5. A driver circuit as claimed in any one of Claims 1 to 3, in which the maximum current (I_{max}) through the paths (2,4,6;10,Q_B,Q_M,12) is limited indirectly by the maximum current (I_O) through the output portion (23) of the current mirror. 25
6. A driver circuit as claimed in Claim 5, in which current (I_{lim}) through the paths (2,4,6;10,Q_B,Q_M,12) passes through gating means (Q11) which is gated by the current (I_O) through the output portion (23) of the current mirror. 30
7. A driver circuit as claimed in Claim 6, in which the gating means is a transistor (Q11). 35
8. A driver circuit as claimed in Claim 6 or Claim 7, in which the circuit comprises signal generation means (30,Q2,Q3,Q4,Q5,Q6) to compensate for gain variability of the gating means (Q11). 40
9. A driver circuit as claimed in any preceding claim, in which the circuit comprises signal generation means (11,12,Q4,Q5,Q6) to compensate for temperature variability of the optical emitter (8) optical power versus temperature characteristic. 45
10. A driver circuit as claimed in Claim 8 or Claim 9, in which the first current (I_R) through the input portion (21) of the current mirror passes through at least one transistor (Q6) which is gated by the signal generation means. 50
11. A driver circuit as claimed in any preceding claim, in which the current return path (10,Q_B,Q_M,12) has bias control means (Q_B) to set a bias current through the optical emitter (8). 55
12. A driver circuit as claimed in any preceding claim, in which the current return path has modulation means (Q_M) to modulate the current through the optical emitter (8).
13. An optical fibre transmission device comprising a laser diode (8) and a driver circuit arranged to drive the laser diode, in which the driver circuit is as claimed in any preceding claim.
14. A method of driving a solid state optical emitter (8) with a circuit comprising a current supply path (2,4,6) and a current return path (10,Q_B,Q_M,12) to which optical emitter (8) may be connected, and current limit means (20) to limit a maximum current that may flow through one of the current paths (2,4,6;10,Q_B,Q_M,12), characterised in that the current limit means (20) has a current mirror (Q9,Q10), comprising the steps of:
 - i) generating a first current (I_R) in an input portion (21) of the current mirror;
 - ii) predisposing an output portion (23) of the current mirror to supply a second current (I_O) up to a maximum which mirrors the first current (I_R); and
 - iii) using the maximum second current (I_O) to limit the maximum current (I_{max}) through the paths (2,4,6;10,Q_B,Q_M,12).

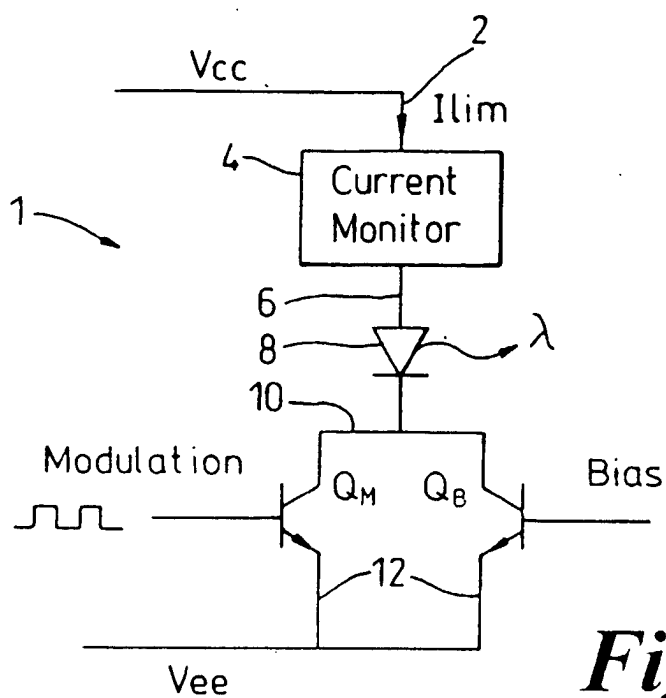


Fig. 1

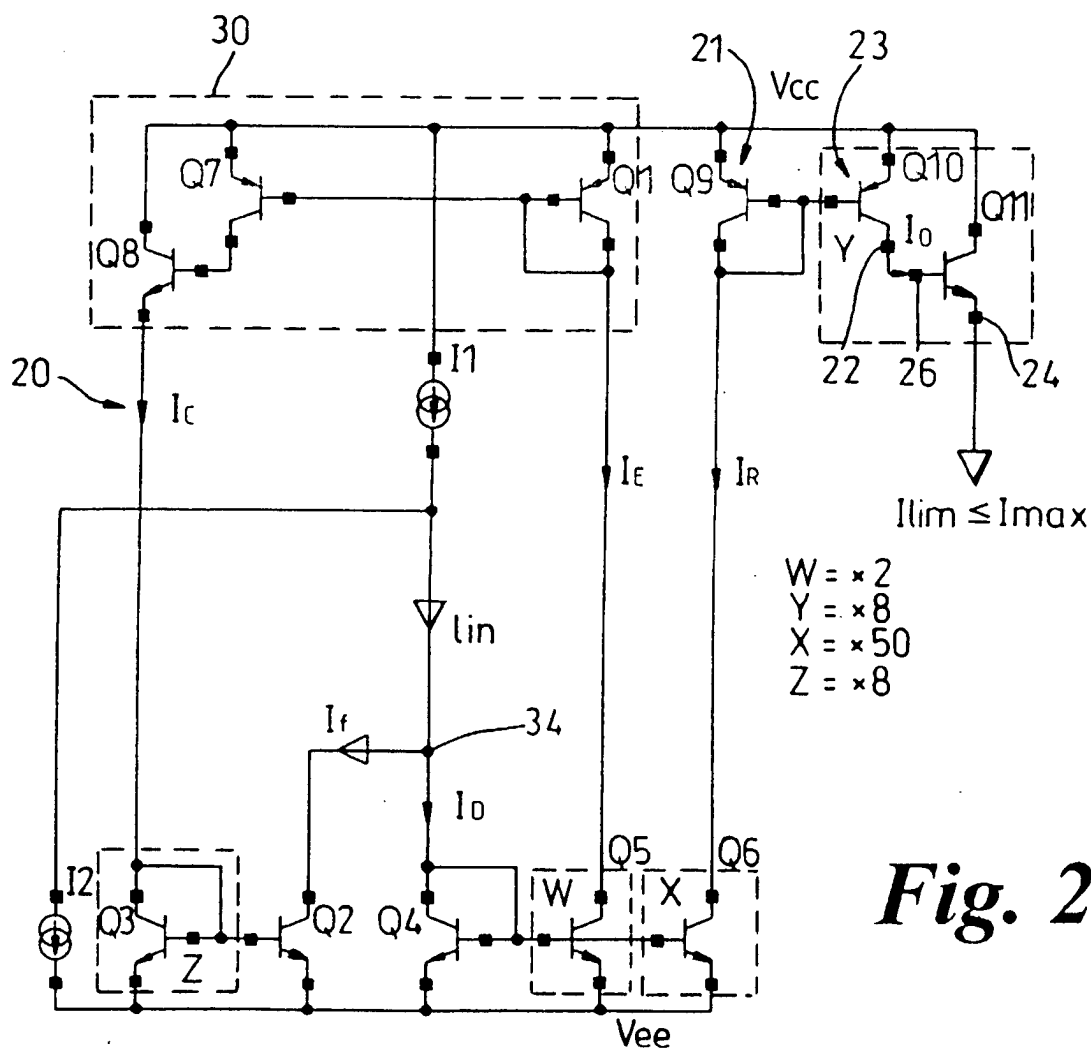


Fig. 2

EP 0 924 823 A1

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EUROPEAN SEARCH REPORT

Application Number
EP 97 31 0246

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X A	EP 0 563 580 A (CANON KK) 6 October 1993 * figures 9,10 *	1-3,14 4.5	H01S3/096 H05B33/08
X	--- PATENT ABSTRACTS OF JAPAN vol. 012, no. 063 (E 585), 25 February 1988 & JP 62 206893 A (TOSHIBA CORP), 11 September 1987, * abstract *	1,14	
A	--- PATENT ABSTRACTS OF JAPAN vol. 095, no. 004, 31 May 1995 & JP 07 007204 A (MITSUBISHI ELECTRIC CORP), 10 January 1995, * abstract *	3,11,12	
A	--- PATENT ABSTRACTS OF JAPAN vol. 095, no. 004, 31 May 1995 & JP 07 007204 A (MITSUBISHI ELECTRIC CORP), 10 January 1995, * abstract *	1,11,12, 14	
A	--- EP 0 603 899 A (CANON KK) 29 June 1994 * figures 1,2 *	1,6,7,14	
A	--- EP 0 589 397 A (HITACHI LTD) 30 March 1994 * abstract: figure 1 *	1,11-13	
A	--- PATENT ABSTRACTS OF JAPAN vol. 013, no. 248 (E-770), 9 June 1989 & JP 01 049290 A (MITSUBISHI ELECTRIC CORP), 23 February 1989, * abstract *	1	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01S H05B
A	--- PATENT ABSTRACTS OF JAPAN vol. 013, no. 354 (E-802), 8 August 1989 & JP 01 114091 A (MITSUBISHI ELECTRIC CORP), 2 May 1989, * abstract *	1,9	
The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 22 May 1998	Examiner Claessen, L
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document			

**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 97 31 0246

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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22-05-1998

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0563580 A	06-10-1993	JP 5243654 A	21-09-1993
		DE 69311755 D	31-07-1997
		DE 69311755 T	08-01-1998
		EP 0704948 A	03-04-1996
		US 5349595 A	20-09-1994
EP 0603899 A	29-06-1994	JP 6196746 A	15-07-1994
		US 5514989 A	07-05-1996
EP 0589397 A	30-03-1994	JP 6112561 A	22-04-1994
		US 5675599 A	07-10-1997